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PATENT

#14 Dillon 5-6-03 Appeal Brief

ON APPEAL TO THE U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant	:	Stuart I. Hodge, Jr.	Examiner:	Gary Laxton
Serial No.	:	09/749,354	Art Unit:	2838
Filed	:	12/27/2000		
For	:	Method and Circuitry for Active Inrush Current Limiter and Power Factor Control		

APPELLANT'S BRIEF

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This is Appellant's Brief on Appeal pursuant to 37 C.F.R. § 1.192.

37 C.F.R. §§ 1.92(c)(1)-(7)

Real Party in Interest

Ascom Energy Systems, AG, a Swiss corporation and assignee of the inventor Stuart I. Hodge, Jr., is the real party in interest.

Related Appeals and Interferences

There are no related appeals or interferences.

Status of Claims

Claims 1 - 11 and 13 - 22, all of the claims in this application are the claims on appeal. Each of claims 1 - 11 and 13 - 22 are under final rejection. The claims on appeal are appended at Appendix A.

Status of Amendments

No amendment has been filed subsequent to the Official Action dated September 5, 2002.

Summary of the Invention

The invention is an improvement that protects against high amperage "inrush" currents in power supply circuits. A control output of a controller that is part of an active power factor correction circuit (84 in Fig. 3, 32 in Fig. 4A) controls a bypass switch transistor (82 in Fig. 3, Z1 in Fig. 4A) in an inrush current limiting circuit. (This is the circuit 82 and 83 in Fig. 3, and in Fig. 4A, Z1 and the positive temperature coefficient resistor PTC). For convenience, appellant's drawings are appended as Appendix B.

When a power supply is turned on, a tremendous high and potentially damaging current can be drawn by, for example, capacitance at the output of the circuit. In one inventive embodiment, the bypass switch 82 or Z1 of this application is connected in parallel with a passive resistive current limiting element 83 or positive temperature coefficient resistor (PTC). This resistive element limits the inrush current until the switch is turned on by the controller of the power factor control circuit (84 in Fig. 3 or 31 in Fig. 4A). The switch is turned on by the power factor control circuit controller when it senses that the inrush current (sensed at R_{sns} in Figs. 4A, 4B and 5) has subsided. This occurs when an output capacitor (C_{out} in Figs. 4A, 4B and 5) has been fully or nearly fully charged.

The invention includes the method of limiting inrush current (Fig. 7). The steps of the method include passively controlling inrush current (at 70) with a passive device while an inrush current condition exists (at 68) and then using a power factor control signal (at 63) to actively control current (at 64) by shunting the current past the passive device (at 65).

The power factor control circuit that generates the signal that activates the switch to end the limiting of current can be a commercially available integrated circuit (UPFC 46 of Fig. 5). The switch can be an insulated gate bipolar transistor (IGBT) operated from a gate driver (d1, d2 Fig. 4A, d3, d4 Fig. 5) that is controlled by the signal (Gate in Fig. 4A, 4B, DRIVE in Fig. 5) from the power factor control circuit.

This invention addresses inrush current protection in a manner that solves many weaknesses in previous designs. First, because it uses a power factor correction controller, the circuit has knowledge about the very condition the circuit seeks to control, i.e. current. The current sensing capabilities and the inherent over-current protection within the controller also control the inrush protection circuit. Simply put, the pulsing output from the controller stops pulsing if it senses an over-current condition. That normally just protects the main power factor

correction switch. By this invention, that same condition turns off the active switch in the inrush circuit. The inventive circuit is inexpensive and easy to implement because the control is already part of the power factor correction design and it is robust.

The Issues

Claims 1 and 7 stand rejected as anticipated by U.S. patent No. 5,930,130 to Katyl et al. under 35 U.S.C. § 102. Claims 2 - 6 stand rejected as obvious over Katyl et al. under 35 U.S.C. § 103(a). Claims 8 - 11 and 13 - 22 stand rejected as obvious over Katyl et al. in combination with U.S. patent No, 5,420,780 of Bernstein et al.

These rejections raise the following issues:

1. Does the Katyl et al. patent teach the use of a control signal generated by a power factor control circuit, integrated circuit or "controller" to control a switch in an inrush current control circuit as claimed.

2. Would the Katyl et al. patent have made obvious the claimed circuitry of dependent claims 2 - 6 in the absence of the control of an inrush circuit switch by a power factor controller signal as claimed in independent claim 1.

3. Would the combination of the Katyl et al. and Bernstein et al. patents have made obvious the apparatus and methods of claims 8 - 11 and 13 - 22 in the absence of any prior art teaching of the claimed control of a switch or switching transistor by a power factor control IC or "controller" output signal.

Grouping of Claims

The claims in this application do not stand or fall together.

Argument

The primary reference of each outstanding rejection, the Katyl et al. patent, relates to a ballast circuit for fluorescent lamps. It does include a power factor correction circuit and inrush protection.

The Katyl et al. patent recognizes the need for an inexpensive inrush current protective arrangement. Like the circuit of the present invention, it is intended to initially pass inrush current through a current limiting resistor 30 in Fig. 3C. When the inrush current condition is believed to have subsided, it turns on a bypass switching MOSFET 31. Katyl et al. take the supply voltage (what one would ordinarily call the bias voltage Vcc) at line 26 to the power factor control integrated circuit 14 in Fig. 2 and they apply it to the MOSFET 31, in Fig. 3C. The patent notes that the component count is low for this arrangement, giving the desired cost savings. This is also an advantage of the invention on appeal. Katyl et al. note that the power factor correcting IC supply voltage on line 26 will ordinarily rise sufficiently slowly to timely control the MOSFET switch, i.e. allowing inrush current to subside. Katyl et al. do not however recognize that a control output from the power factor control IC could be used to better control a bypass switch in an inrush current protective circuit. The circuit that Katyl et al. use to apply the IC supply voltage to the inrush current protective MOSFET is an RC timing circuit. Appellant attaches a copy of Katyl et al.'s Figs. 2 and 3C as Appendix C hereto. An unnumbered resistor and capacitor have been designated R_1 and C_1 on the attached. It is the time that it takes the capacitor C_1 to charge to a level sufficient to turn on the inrush protective MOSFET 31 in Fig. 3C that determines when that MOSFET will turn on, not the level of the actual inrush current. Katyl et al. rely on the inrush condition being over by the time the capacitor C_1 has charged sufficiently to turn on the MOSFET 31.

Central to all outstanding rejections in this application is the examiner's misunderstanding that in the Katyl et al. patent a power factor correction integrated circuit 14 (Fig. 2) applies a signal to control an active element or switch 31 (Fig. 3C) in an inrush suppression circuit (27 in Fig. 2, 70 in Fig. 3C). It does not.

Each of the independent claims in this application, claims 1, 9 and 15, requires use of the controller or the application of the control signal from the power factor control circuit to control the inrush current controlling provisions of the circuit.

Claim 1:

> the active power factor correction circuit having a controller; and the inrush control circuit comprising at least one switch having a control element coupled to a control output of the controller.

Claim 9:

> generating a power factor control signal; and implementing the power factor control signal to actively control the inrush current, wherein the step of actively controlling the inrush current shunts output current around the passive device and through an active device.

Claim 15:

> the controller adapted to controlling: a power factor correction control circuit; an active current limiting device, ...

In the Katyl et al. patent, biasing of the gate of a MOSFET 31 in Fig. 3C controls conduction through the MOSFET, either by-passing a resistor 30 or, when open, directing current through the current limiting resistor 30. This arrangement the appellant has acknowledged as not being new. The Katyl et al. circuit, however, does not use a signal from a power factor control (PFC) controller to turn the MOSFET on and off. To control the inrush current MOSFET 31, the Katyl et al. circuit uses a voltage on lines designated 26 in Figs. 2 and 3C. At column 3, lines 44 - 47, Katyl et al. explicitly describe that signal:

> Signal 26 is the supply voltage used to provide power to the IC 14 via a bootstrap rectifier 26' connected to the secondary of inductor 15.

That this is accurate is very apparent from Fig. 2 of the Katyl et al. patent as well. Katyl et al. go on to say:

> In the case of a boost PFC [power factor control] circuit as described in FIG. 2, the control of the MOSFET 31 is realized by simply connecting the MOSFET gate lead to IC supply voltage 26. This voltage typically rises sufficiently slowly so that the MOSFET 31 is held in the OFF state during the inrush interval, and turns ON to short out resistor 30 before the PFC IC 14 is activated. Also, the IC voltage 26 has a magnitude selected to control the gate without exceeding the maximum allowable voltage (typically 20 volts). This is due to the fact that the voltage is selected to match the requirements of the PFC switch MOSFET 17 (FIG. 2).

Column 4, lines 36 - 46. By teaching that the IC supply voltage at 26 "rises sufficiently slowly so the MOSFET 31 is held in the OFF state during the inrush interval ...," the Katyl et al. patent teaches against the use of an IC-developed signal as the MOSFET control. No other art of record in this application counters that teaching of Katyl et al. in this respect. Note that "the MOSFET 31 ... turns on to short out resistor 30 before the PFC IC 14 is activated." If the PFC has not yet

been activated it cannot supply the control signal to turn on the bypass MOSFET 31 as the examiner contends. It isn't operative!

In the final rejection of September 5, 2002, at paragraph 7, "Response to Arguments," the examiner refers to Col. 4, lines 53 - 55 to support his mistaken understanding that the power factor control IC controls the bypass MOSFET 31. There the patent states, "Existing signals within the PFC 14 are used to control the switching of MOSFET 31." To the extent that this statement suggests control of the MOSFET 31 by the power factor control IC 14 (which is not what the statement says) it is wrong. The circuit diagram of Figs. 2 and 3C and the detailed explanation of the use of the IC 14's supply voltage at lines 26 of the circuit clearly and unequivocally state that the MOSFET 31 is controlled from the input or "supply voltage", not a control signal from the IC 14. If what the patentees Katyl et al. mean is that the voltage at 26 is one used by the IC 14, this is correct. But that is because it is a "supply voltage" on which the IC 14 runs. It is not a control signal or output developed by the IC 14 like that applied to the MOSFET 17 of the power factor control circuit. The IC 14 of Katyl et al. simply plays no part at all in control of the inrush current suppressing circuit or the bypass MOSFET 31. Only if read in a vacuum, without reference to the circuit diagrams of Figs. 2 and 3C, and without reading the express, explicit explanation of the use of voltage at 26 at col. 4, lines 36 - 46, could the patentees' comment at lines 53 - 55 of column 4 be misunderstood to suggest that the power factor control IC 14 or a control signal generated thereby controls the inrush circuit's bypass MOSFET 31. Read in its entirely the Katyl et al. patent is unambiguous and there is no way the circuit diagrams of Figs. 2 and 3C can be understood to operate as suggested in the outstanding rejections.

Appellant's invention is simple and robust because it does not rely upon a timing circuit to decide when the bypass switching transistor Z1 should be turned on. Appellant's inventive circuit relies on the actual current under control, which is what a PFC IC responds to. Unlike Katyl et al., appellant's power factor control IC is up and running when the bypass switching transistor Z1 is turned on; the IC itself turns Z1 on. Rather than waiting a predetermined amount of time until it is assumed that inrush conditions will have subsided as Katyl et al. teach, by using the power factor correction circuit's own over-current protective capability, the appellant's circuit turns on the bypass transistor Z1 when current reaches an acceptable level and turns off the transistor Z1 when the current limiting of the parallel resistive path is called for. An advantage of this more direct approach over Katyl et al. is that the appellant's circuit cannot be fooled into

thinking that there is no inrush condition. The inrush current protection of the present invention solves weaknesses in prior designs, ones like Katyl et al.'s. On occasion of a loss of one or two cycles of AC power, or even less, the Katyl et al. capacitor C_1 as shown in Appendix C will not discharge completely. It will hold up the voltage at line 26. In such an intermittent occurrence, when the input AC comes back up, a harmful inrush current can occur, but Katyl et al.'s bypass MOSFET 31 will still be turned on by the voltage across capacitor C_1. Because appellant's power factor control circuit control signal is used to control the bypass transistor in the appellant's invention, this does not occur. No RC circuit is relied upon. No capacitor holds up the voltage of the power factor correction signal. When AC input is briefly interrupted, even for the shortest duration, the inrush protective circuit of the invention does not have to wait for a capacitor to discharge. The switching transistor Z1 is instantly switched off. Likewise, just as soon as the inrush condition subsides, the bypass transistor Z1 of the invention is immediately switched on by the power factor control circuit controller signal, not at a time when a capacitor in an RC circuit has charged to a desired voltage. The circuit's responsiveness to current conditions is what provides the robustness of the circuit of this invention. Timing circuits are not required and delays associated with mechanical devices have been avoided.

Anticipation

Claims 1 and 7

Rejected as anticipated by the Katyl et al. patent, under 35 U.S.C. §102(b), both of claims 1 and 7 are patentable over that patent. Unlike the Katyl et al. patent, claim 1 calls for the inrush control circuit "comprising at least one switch having a control element coupled to a control output of the controller." (Emphasis added.) Claim 7 is dependent from claim 1 and so includes that limitation by its dependency.

For a rejection of a claim to be appropriately rejected as "anticipated" under 35 U.S.C. §102, it is well established that every element of the claim must appear in the relied-upon prior art citation. *Gechter v. Davidson*, 116 F.3d 454, 1457, 43 U.S.P.Q (BNA) 2d 1030, 1032 (Fed. Cir. 1997), for example. Since the Katyl et al. patent does not meet the above-quoted limitation, i.e. does not have, in an inrush control circuit, "at least one switch having a control element coupled to a control output of the controller," the rejection of claims 1 and 7 over the Katyl et al. patent is in error and should be reversed.

Obviousness

In none of the obviousness rejections here on appeal has the examiner made out a prima facie case of obviousness as required. It is necessary, for a determination of obviousness, to ascertain whether or not the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art, having the references before him or her, to make the substitution, combination or other modification. *In re Lintner*, 458 F.2d 1013, 1016, 173 U.S.P.Q. (BNA) 560 (CCPA 1972). Here, because no reference of record teaches an essential claim limitation, the references alone or in combination do not suggest the missing limitation and hence prima facie obviousness has not been made out. *In re Fritch*, 972 F.2d 1260, 1265, 23 U.S.P.Q. 2d (BNA) 1780, 1783 (Fed. Cir. 1992). Of course the claim limitation missing from all art of record is, as discussed above, the use of the power factor correction controller's control output signal to control the bypass switch of the inrush protection circuit.

It is also true that for obviousness to be established there must be some suggestion, teaching or motivation for the modification that is asserted to be obvious. Even when obviousness is based on a single reference this is true. *In re Kotzab,* 217 F.3d 1365, 1370, 55 U.S.P.Q. 2d (BNA) 1313, 1316-17 (Fed Cir. 00). Here no such suggestion appears in the prior art for modifying the Katyl et al. circuit to meet the terms of the claims.

Claims 2 - 6

Claims 2 to 6 stand rejected as obvious over Katyl et al. standing alone. Each of these claims is dependent from claim 1 or from a claim or claims dependent from claim 1. Each rejection of claims 2 - 6 relies upon and incorporates the misunderstanding of the Katyl et al. patent discussed fully above. Even if the further features of the invention set forth in claims 2 - 6 were obvious as the examiner contends, there is still no teaching of the control of a switch in an inrush current control circuit by a controller in an active power factor correction circuit. These claims are not properly rejected as obvious over the Katyl et al. patent which never teaches or suggests this feature. The Inn et al. patent, made mention of in the rejection of claims 4 - 6 for a teaching of gate/driver circuits, does not overcome the failing of Katyl et al. in this respect.

Claims 8 - 11 and 13 - 22

As with the obviousness rejections of claims 2 - 6, the examiner again premises his rejection of claims 8 - 11 and 13 - 22 on the misperception that the Katyl et al. patent discloses control of the bypass MOSFET 31 from the controller IC 14 of Katyl et al. This premise is in error for the reasons stated above. The secondary Bernstein et al. patent is similarly deficient. It is cited to allegedly supply a teaching of other recitations of the rejected claims 8 - 11 and 13 - 22. No combination of the Katyl et al. and Bernstein et al. teachings will result in the claimed invention since neither teaches the claimed switch control as described above and claimed in all of these claims. Again, the Inn et al. patent noted by the examiner in passing, in the rejection of claims 8 - 11 and 13 - 22 does not supply the claim feature missing from Katyl et al. and Bernstein et al. For these reasons the invention as set forth in claims 8 - 11 and 13 - 22 would not have been obvious from Katyl et al., Bernstein et al. and Inn et al., taken individually or combined. This rejection, too, is in error and should be reversed.

As for the particular claims, claim 8 is dependent from claim 7, which is dependent from claim 1, and is patentable over Katyl et al. as described above.

Claim 9 is an independent method claim that spells out, as quoted above, "implementing the power factor control signal to actively control the inrush current." Again, no art of record teaches this and Katyl et al. teach away from this as previously discussed.

Claims 10, 11, 13 and 14 are dependent claims, incorporating by their dependency the limitations of claim 9 and patentable over the prior art of record for that reason.

Claim 15 is an independent apparatus claim that makes it clear, as quoted above, that the "controller" is "adapted to controlling" the power factor correction control circuit and the active current limiting device. Again, this distinguishes the Katyl et al. patent, the Bernstein et al. patent and the Inn et al. patent as discussed above.

Claims 16 - 22 by their dependency include the limitations of claim 15 and are patentable therewith.

Conclusion

For the reasons expressed above, appellant respectfully urges that each of the claims now pending in this application patentably differ from the art cited. Reversal of the

outstanding rejections and allowance of the application at this time is appropriate.

Respectfully submitted,

GALLAGHER & KENNEDY

Date: 03/03/03

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